SPECIFICATION

COMPUTER-SUPPORTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT

Background of the Invention

In circuit simulation of very large circuits, i.e. of circuits having a great plurality of elements, a serial processing, i.e. the determination of the circuit quantities by a computer, is extremely time-consuming. Even vector computers that are very expensive in terms of operation have an immense need of calculating capacity and time for determining the electrical descriptive quantities for a circuit that comprises a few 100,000 transistors.

In order to avoid the serial implementation of a circuit simulation for this reason, the electrical circuit can be divided into a plurality of parts that are then respectively processed by different computers or, respectively, processors, this leading to a parallel implementation of the circuit simulation.

In order, however, to achieve an optimally good parallelization of the determination of the electrical descriptive quantities for the electric circuit, it is advantageous to consider the following two criteria in the partitioning of the electrical circuit into a plurality of parts. ~~It is~~ First, it is of considerable significance that all partitions of the electrical circuit that are formed are of the same size insofar as possible, in order to thereby intensify the effect that can be achieved by the parallelization. When, for example, one partition is orders of magnitude larger than the remaining partitions, then the processing of the significantly larger partition is in turn far more calculation-consuming then the processing of the remaining partitions. ~~Further,~~ Second, it is important in the partitioning that only a slight plurality of connections exists between the individual partitions insofar as possible since, in known methods for "parallelized" circuit simulation, the required transmission capacity, i.e. the required communication between the computers or, respectively, processors that respectively process one partition, increases substantially with an increasing number of existing connections between the partitions.

A language for textual description of an electrical circuit that can be processed by a computer is known from document [1] as circuit simulation language SPICE.

Documents [2] and [3] describe how a parallelized circuit simulation can be implemented, assuming an arbitrary number of partitions of the electrical circuit exist. The way in which the partitions can be determined is not described in these documents.

Document [4] discloses a global partitioning method on what is referred to as the logic level, which is also referred to as gate level.

Discrete events are described on the logic level, but no steady dynamic property of an electrical circuit on what is referred to as the transistor level, i.e. on the actual physical level of the electrical circuit, can be described with these.

The results of a circuit simulation that ensues on the logic level is thus unreliable and imprecise for certain applications since an exact time course of the electrical signals that occur in the electrical circuit cannot be taken into consideration.

Further, a description of the individual gates is required for the circuit simulation, this having to be determined first before the method can be implemented.

An overview of various partitioning rules can be found in [5].

A parallelized method for clustering an electrical circuit according to what is referred to as the bottom-up principle is disclosed by [6].

The present invention provides The method [sic] is thus based on the problem of specifying a method for partitioning an electrical circuit that directly considers the elements of the electrical circuit on the transistor level.

The problem is solved by the method according to patent claim 1.

In the method, the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit. The edges of the graph are weighted with weighting values that describe in approximately required calculating outlay for determining electrical descriptive quantities for the element of the electrical circuit respectively represented by the edge. A

partition for the electrical circuit is formed in the graph in that edges coupled with one another are combined to form the partition at the beginning of the method until the sum of the weighting values of the combined edges is greater than a first, prescribable threshold. When the first threshold is reached, the partition is then respectively expanded by further, remaining edges when the sum of the weighting values of all edges, including the edges to be potentially newly added, is smaller than a prescribable, second threshold, and when the plurality of edges of the partition that are connected to nodes that do not lie within the partition is reduced by the addition of at least one new edge.

The method exhibits a number of substantial advantages compared to the method disclosed by ~~document [4].~~

Since the method works directly of the transistor level of the electrical circuit, the results achieved by the method are substantially more exact and dependable given a later circuit simulation ~~upon employment~~ employing of the partitions that have been ~~inventively~~ determined in accordance with the invention.

~~Advantageous developments of the invention derive from the dependent claims.~~

For prescribable elements of the electrical circuit, it is advantageous to determine at the beginning of the method that the elements are grouped in common into a partition. As a result of this development of the method, it becomes possible to assure that, for example given controlled sources, both the controlling elements as well as the controlled source can be processed in common in one partition. This development also makes it possible to likewise allocate connecting leaps in the electrical circuit that only comprise at least one voltage source and/or at least one inductance in common in one partition. This procedure also makes it possible to avoid shorts that may potentially occur due to the partitioning.

Due to the development of the method that a plurality of edges of the graph have a common weighting value allocated to them, the implementation of the method is further accelerated by a computer since, given this

development, a lower number of weighting values must be taken into consideration during the course of the method.

It is also advantageous to form a plurality of partitions for the electrical circuit, to again image the corresponding graphs of the partitions onto the electrical circuit for the partitions, and to process the arising partitions of the electrical circuit in parallel on different computers or, respectively, processors. As a result of this parallelization, a circuit simulation of an extremely large circuit can be implemented significantly faster then given a purely "serial" circuit simulation.

It is also advantageous in the parallelized circuit simulation, to control the processing of the individual partitions centrally. In this way, a controlled circuit simulation is realized with optimally low communication outlay.

It is also advantageous to additionally provide the individual terminals of the partitions that are coupled to components that do not lie in their partition with a voltage source and a resistor, whereby the voltage source has the electrical boundary descriptive quantities respectively allocated to it by a central control unit that controls the parallelized processing of the partitions. As a result of the resistor that is respectively provided in the terminals, the convergence of the circuit simulation is assured during the parallelized circuit simulation, the value thereof being dynamically adapted by the control unit.

~~The Figures show an exemplary embodiment of the method that is explained in greater detail below.~~

~~Shown are:~~

Fig. 1 a flow chart wherein the individual method steps of the method are shown;

Fig. 2 a sketch that shows various developments of the method.

~~Electrical~~ circuits that comprise an extremely great plurality of elements can be parallelized into an arbitrary plurality of partitions and a processing of the individual partitions on different computers or, respectively, processors that implement a circuit simulation. The implementation of the overall circuit simulation can thus be considerably speeded up.

In order for the parallelization, however, to be designed as optimally as possible, the individual partitions must be carefuily defined.

It is thereby important, first to make sure of an approximately uniform size of the partition and, second, to make sure that the individual partitions do not comprise an excessively great plurality of terminals "toward the outside", for example couplings to other elements not lying in the partition.

Electrical circuits for processing within the framework of a circuit simulation by a computer are usually present in a circuit description language 101, for example in what is referred to as the language SPICE, which is described in ~~the document [1].~~

The method, however, is definitely not limited to a description of the electrical circuit in a circuit description language and is likewise not limited to the employment of the specific circuit description language SPICE.

With reference now to the figures, in ~~In~~ a first method step 102, the electrical circuit is imaged ~~on~~ onto a graph that exhibits the same topology as the electrical circuit. This ensues, for example, proceeding from the electrical circuit present in the circuit description language SPICE. The graph comprises the corresponding nodes corresponding to the topology of the electrical circuit. The individual elements of the electrical circuit are represented by edges between the nodes of the graph.

It is advantageous in a development of the method to mark individual elements of the electrical circuit at the beginning of the method, i.e. to determine for the corresponding, marked elements that the marked elements are respectively allocated in common to one partition in the further method. Various markings can assign various elements to different partitions. It is also provided to mark elements only in a way that is interpreted such by the computer that implements the method that the respectively paired elements are allocated to one partition.

It is thereby advantageous, for example, to take the following specific instances of an electrical circuit into consideration. When an electrical circuit contains controlled sources, for example controlled current sources or controlled voltage sources, then it is advantageous that both the controlling

elements as well as the controlled source are contained in common in one partition for the later circuit simulation.

It is further advantageous to likewise allocated coupled inductances to a common partition. It is also important to take into consideration in a development of the method that no shorts dare occur due to the partitioning and the algorithmic processing thereof with a computer.

In a further step 103, weighting values G are allocated to the edges. The weighting values G describe what calculating outlay is approximately expected for determining electrical descriptive quantities for the respective element of the electrical circuit that is represented by the edge to which the weighting value G is respectively assigned.

One criterion for the required calculating outlay is to be seen, for example, in the plurality of code lines required for determining the electrical descriptive quantities for the respective, specific element within the framework of the circuit simulation. It should be noted here as a rough rule that the determination of the electrical descriptive quantities for transistors is substantially greater than the outlay for determining the electrical descriptive quantities for an electrical resistor or for a capacitor as well. The selection of the weighting values G, however, ~~is basically uncritical~~ basically is not critical and merely represents an approximate size relationship of the required calculating outlay. It is even adequate to allocate a high weighting value G, for example, the weighting value G = 300 to, for example, an edge that represents a transistor and to allocate a low weighting value, for example a weighting value G =1 or even a weighting value G = 0, to the edges that represent a resistor or a capacitor.

What are to be understood as electrical descriptive quantities in this conjunction are, for example, the corresponding currents and voltages of an element of the electrical circuit.

A first iteration loop implemented thereafter contains the following method steps.

~~An~~ An arbitrary edge of the graph is selected 104 at the beginning of the first iteration loop. However, it is likewise provided in one version of the

method to select an arbitrary plurality of edges of the graph coupled to one another in this method step, as a result whereof the number of required iterations in the first iteration loop 105, 106, 107 is substantially reduced. Two method steps 106, 107 described later are implemented, proceeding from the selected edge or, respectively, proceeding from the set of selected edges, until the first sum value SW1 is greater than a freely prescribable, first threshold S1.

The first sum value SW1 is formed for respectively at least one new edge that was not contained in the set of considered edges from the last iteration or, respectively, that was not contained in the selected set of edges at the beginning of the first iteration loop. The first sum value SW1 is formed, for example, by summation of the weighting values G of all of the edges that are utilized 106 for the formation of the first sum value SW1.

When the first sum value SW1 is not greater then the first threshold S1, a partition of the electrical circuit derives from the edges that were utilized 107 for the formation of the first sum value SW1, and the method steps of the first iteration loop are re-implemented, now with the "new" partition.

When, however, the first sum value SW1, is greater then the first threshold S1, then the partition formed in the iteration step preceding in time is employed, and method steps of a further, second iteration loop are implemented for the partition that is formed.

Proceeding from the respective partition, the following method steps designated 108 are implemented ~~108~~ in each iteration step of the second iteration loop for at least a part of the remaining edges of the electrical circuit. What is to be understood by a remaining edge in this context is an edge that is not already contained in the partition itself and that is coupled to an edge that is contained in the partition, for example via a node in the partition.

A second sum value SW2 is formed at 109 from the weighting values of the partition and the weighting values of at least one additional, remaining edge. This ensues, for example, by simple summation over the weighting values G allocated to the corresponding edges.

A check is now carried out to see whether the second sum value SW2 that has been formed is greater than a freely prescribable, second threshold S2 that is higher than the first threshold S1, at 110.

When the second sum value SW2 is greater then the second threshold S2, then this means that the partition is larger than a prescribable region that can be tolerated. A tolerance region for the size or, respectively, for the maximum required processing outlay that can be tolerated in the circuit simulation of the respective partition is thus described by the first threshold S1 and by the second threshold S2.

When, thus, the second sum value SW2 is greater than the second threshold S2, then the corresponding edge is not added, at 111 to the partition.

When, however, the second sum value SW2 is not greater then the second threshold S2, then a further check is carried out for the at least one remaining edge to see whether a plurality of edges that were taken into consideration in the formation of the second sum value SW2 and that are coupled to edges that were not taken into consideration in the formation of the second sum value SW2 is smaller than a plurality of edges of the partition that are coupled, at 112 to the remaining edges.

As can be seen, this comparison corresponds to the plurality of "section points" of every partition with another partition or, respectively, with another element of the electrical circuit as well that is not contained in a partition or, respectively, with a central control unit (described later) ~~[sic]~~.

When, as can be seen, the number of terminals for each partition thus becomes greater - by adding the at least one remaining edge - then the plurality of terminals of the partition that already previously existed, then the corresponding edge is not added, at 113. When, however, the new plurality of terminals has been reduced, then the corresponding, remaining edge is added, at 114 to the partition. For this case, further, the first sum value SW1 for the next iteration of the second iteration loop is occupied with the value of the second sum value SW2.

The second iteration loop is implemented for an arbitrarily prescribable plurality of remaining edges. It is likewise provided in a

development of the method to simply employ the information as to whether all remaining edges have been taken into consideration in the second iteration loop as abort criterion for the second iteration loop. When this is the case, then the second iteration loop is ended in this development. After abort or, respectively, conclusion of the second iteration loop, the partition that was formed in the last iteration of the second iteration loop is employed as partition 116 of the electrical circuit.

Upon employment of the original description of the electrical circuit, for example in the circuit description language SPICE, the partition is imaged into a syntax to be further-processed for the computer, for example again in the circuit description language SPICE. In this imaging, the information of the respective partition for the respective element of the electrical circuit is taken into consideration, for example, by marking the respective element.

As a result of this back-imaging 201 (see Figure 2), thus, a list with the circuit elements of the electrical circuit as well as with the couplings and the respective indication of the partition to which the respective element was allocated in turn arises for the specific cases of employing the circuit description language SPICE.

It is advantageous in a development of the method to implement this method for an arbitrary number of partitions, i.e. the electrical circuit is sub-divided into an arbitrary plurality of partitions. Given this development, partition-specific lists with the elements of the electrical circuit in the circuit description language SPICE arise 202 according to the plurality of partitions formed. A parallelization of the circuit simulation of the electrical circuit that is advantageous in a development of the method is now achieved in that the electrical descriptive quantities for the elements of the electrical circuit are separately identified for each partition, whereby at least a part of the partitions can be processed in parallel on a plurality of computers and/or processors. This corresponds to a parallelization of the circuit simulation.

It is also provided in a development of the method to allocate a common weighting value to a plurality of edges of the graph. The required calculating outlay is reduced as a result of this procedure.

Methods for parallelized circuit simulation on distributed processors or, respectively, distributed computers are known, for example, from the document [2] and [3]. These can be applied without limitation to the partitions formed by the method.

It is also provided in a development of the method to centrally control the parallel processing of the partitions via a central control unit ZS. This means, for example, that the communication of the individual partitions in the method of the circuit simulation as described in documents [2] and [3], i.e. the communication of data ensues only between the central control unit ZS and the part of the partitions that is centrally controlled.

Figure 2 symbolically shows the parallelized processing by a plurality of SPICE data files SPICE.1, SPICE.2, SPICE.3 through SPICE.N. The individual descriptions of the partitions are contained in these SPICE data files in the circuit description language SPICE.

A circuit simulation is implemented 203 for the respective partition, for example centrally controlled by the central control unit ZS.

It is also provided in a development of the method to additionally allocate a voltage source at least to a part of the terminals of the respective partition that is processed in the framework of the parallelized circuit simulation, a corresponding value being respectively allocated to this additional voltage source by the central control unit ZS in the framework of the known method. In order to assure the convergence of the iterative method from document [2] and [3], it is advantageous to additionally provide a resistor at least at a part of the terminals of the respective partitions, the value of said resistor being dynamically adapted by the control unit ZS.

The following publications were cited within the framework of this document:

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[4] B. Riess et al, Partitioning Very Large Circuits Using Analytical Placement Techniques, Proceedings of the 31st ACM/IEEE Design Automation Conference, pp. 646 through 651, 1994

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